Claims

1. A memory module including a non-volatile memory, a dynamic random access memory, a static random access memory and a control circuit that accesses the non-volatile memory, the dynamic random access memory and the static random access memory, comprising:

a dynamic random access memory interface for accessing the dynamic random access memory from a device outside the memory module; and

a static random access interface for accessing the static random access memory.

2. A memory module according to Claim 1, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the static random access memory.

3. A memory module according to Claim 1, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the dynamic random access memory.

4. A memory module according to Claim 1, wherein:

data transfer between the non-volatile memory and the dynamic random access memory is performed according to an instruction via the dynamic random access memory interface.

5. A memory module according to Claim 1, wherein:

data transfer between the non-volatile memory and the

static random access memory is performed according to an instruction via the static random access memory interface.

6. A memory module according to Claim 1, wherein:

in data transfer from the non-volatile memory to the static random access memory or the dynamic random access memory, data acquired by correcting an error is transferred.

7. A memory module according to Claim 1, wherein:

in data transfer from the static random access memory or the dynamic random access memory to the non-volatile memory, an address replacement process is executed.

8. A memory module according to Claim 1, wherein:

a boot program is held in the non-volatile memory.

9. A memory module according to Claim 1, wherein:

data transfer range data showing a range of data transferred from the non-volatile memory to the dynamic random access memory at initial time when operating power is turned on is held in the non-volatile memory.

10. A memory module according to Claim 1, wherein:

the non-volatile memory and the dynamic random access memory have the similar memory size; and

the static random access memory has memory size equal to/smaller than 1/1000 of that of the non-volatile memory.

11. A memory module according to Claim 3, wherein:

the non-volatile memory holds data transfer range data showing a range of a predetermined address region of the

non-volatile memory.

12. A memory module according to Claim 1, wherein:

the data-hold operation of the dynamic random access memory is executed inside the memory module.

13. A memory module according to Claim 11, wherein:

in case data-hold operation is instructed from the device outside the memory module to the dynamic random access memory, the data-hold operation of the dynamic random access memory inside the memory module is stopped.

14. A memory module according to Claim 1, wherein:

access from the device outside the memory module is first preceded;

the data-hold operation of the dynamic random access memory inside the memory module is second preceded; and

data transfer between the non-volatile memory and the static random access memory or the dynamic random access memory is third preceded.

15. A memory module according to Claim 1, wherein:

the dynamic random access memory is synchronous DRAM; and

access to the non-volatile memory and the dynamic random access memory from the device outside the memory module is made via an interface of the synchronous DRAM.

16. A memory module according to Claim 1, wherein:

the non-volatile memory is a NAND flash memory; and

the dynamic random access memory is synchronous DRAM.

17. A memory module according to Claim 1, wherein:

the non-volatile memory is an AND flash memory; and

the dynamic random access memory is synchronous DRAM.

18. A memory module according to Claim 1, wherein:

the non-volatile memory performs error detection, error correction and address replacement.

19. A memory module according to Claim 18, wherein:

a memory array of the non-volatile memory is configured according to NAND configuration.

20. A memory module according to Claim 18, wherein:

a memory array of the non-volatile memory is configured according to AND configuration.

21. A memory module according to Claim 1, wherein:

the dynamic random access memory is equipped with plural interfaces.

22. A memory module according to Claim 21, wherein:

the plural interfaces with which the dynamic random access memory is equipped are memory interfaces for connecting to at least two types of different memories.

23. A memory module according to Claim 21, wherein:

the interfaces with which the dynamic random access memory is equipped are the dynamic random access memory interface and the non-volatile memory interface.

24. A memory module according to Claim 1, wherein:

the dynamic random access memory is equipped with a control circuit for processing access from the device outside the memory module and a control circuit for independently accessing the non-volatile memory.

25. A memory module according to Claim 1, wherein:

the dynamic random access memory is equipped with a control circuit for independently accessing the non-volatile memory and a circuit for subordinately processing the access.

26. A memory module according to Claim 25, wherein:

the dynamic random access memory can select independent access to the non-volatile memory or subordinately processing the memory access.

27. A memory module according to Claim 1, wherein:

the non-volatile memory is equipped with a static random access memory, an error detecting and correcting circuit and an address replacement circuit.

28. A memory module according to Claim 1, wherein:

the non-volatile memory is equipped with plural interfaces.

29. A memory module according to Claim 28, wherein:

the plural interfaces with which the non-volatile memory is equipped are memory interfaces for accessing at least two types of different memories.

30. A memory module according to Claim 29, wherein:

the interfaces with which the non-volatile memory is

equipped are the non-volatile memory interface and the static random access memory interface.

31. A memory system, comprising:

a memory module including a non-volatile memory, a dynamic random access memory, a static random access memory and a control circuit that accesses the non-volatile memory, the dynamic random access memory and the static random access memory; and

an information processing device, wherein:

the information processing device transfers data to/from the static random access memory in the memory module via a static memory interface and transfers data to/from the dynamic random access memory in the memory module via a dynamic random access memory interface.

32. A memory system according to Claim 31, wherein:

the information processing device reads a boot program from a boot program region of the static random access memory in the memory module via an SRAM interface in an initialization period immediately after power is turned on.

33. A memory system according to Claim 31, wherein:

in a normal period, the information processing device accesses the dynamic random access memory in the memory module via the dynamic random access memory interface and accesses a buffer region of the static random access memory in the memory module via the static random access memory interface.

34. A memory system according to Claim 31, wherein:

the information processing device instructs data transfer between the dynamic random access memory in the memory module and the non-volatile memory via the dynamic random access memory interface; and

the information processing device instructs data transfer between a buffer region of the static random access memory in the memory module and the non-volatile memory via the static random access memory interface.

35. A memory system according to Claim 31, wherein:

in a period when reading, writing, a refresh instruction and other instructions from the information processing device to the memory module are not executed in the memory module, data transfer between the dynamic random access memory and the non-volatile memory is performed and data transfer between the static random access memory and the non-volatile memory is performed.

36. A memory system according to Claim 1, wherein:

the non-volatile memory is formed in a first semiconductor chip;

the control circuit is formed in a second semiconductor chip including the static random access memory;

the dynamic random access memory is formed in a third semiconductor chip; and

the first to third semiconductor chips are a multichip memory module mounted on a circuit board and packaged.

37. A memory system according to Claim 1, wherein:

the non-volatile memory is formed in a first semiconductor chip;

the control circuit is formed in a second semiconductor chip, including the static random access memory;

the dynamic random access memory is equipped with plural interfaces and is formed in a third semiconductor chip; and

the first to third semiconductor chips are a multichip memory module mounted on a circuit board and packaged.

38. A memory system according to Claim 1, wherein:

the non-volatile memory is equipped with plural interfaces and is formed in a first semiconductor chip;

the dynamic random access memory is equipped with plural interfaces and is formed in a second semiconductor chip; and

the first and second semiconductor chips are a multichip memory module mounted on a circuit board and packaged.

39. A memory system according to Claim 31, wherein:

the non-volatile memory is formed in a first semiconductor chip;

the control circuit includes the static random access memory and is formed in a second semiconductor chip;

the dynamic random access memory is formed in a third semiconductor chip;

the information processing device is formed in a fourth semiconductor chip; and

the first to fourth semiconductor chips are a multichip memory module mounted on a circuit board and packaged.

40. A memory system according to Claim 31, wherein:

the non-volatile memory is formed in a first semiconductor chip;

the control circuit is formed in a second semiconductor chip including the static random access memory;

the dynamic random access memory is equipped with plural interfaces and is formed in a third semiconductor chip;

the information processing device is formed in a fourth semiconductor chip; and

the first to fourth semiconductor chips are a multichip memory module mounted on a circuit board and packaged.

41. A memory system according to Claim 31, wherein:

the non-volatile memory is equipped with plural interfaces and is formed in a first semiconductor chip;

the dynamic random access memory is equipped with plural interfaces and is formed in a second semiconductor chip;

the information processing device is formed in a third semiconductor chip; and

the first to third semiconductor chips are a multichip memory module mounted on a circuit board and packaged.

42. A memory system including a memory module including a non-volatile memory, a dynamic random access memory, a static random access memory and a control circuit that accesses the

non-volatile memory, the dynamic random access memory and the static random access memory, comprising:

a dynamic random access memory interface for accessing from a device outside the memory module to the dynamic random access memory and the static random access memory.

43. A memory system according to Claim 42, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the static random access memory.

44. A memory system according to Claim 42, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the dynamic random access memory.

45. A memory system according to Claim 42, wherein:

data transfer between the non-volatile memory and the dynamic random access memory or the static random access memory is performed according to an instruction via the dynamic random access memory interface.

46. A memory system according to Claim 42, wherein:

in data transfer from the non-volatile memory to the static random access memory or the dynamic random access memory, data acquired by correcting an error is transferred.

47. A memory system according to Claim 42, wherein:

in data transfer from the static random access memory or the dynamic random access memory to the non-volatile memory,

an address replacement process is executed.

48. A memory system according to Claim 42, wherein:

a boot program is held in the non-volatile memory.

49. A memory system according to Claim 42, wherein:

data transfer range data showing a range of data transferred from the non-volatile memory to the dynamic random access memory at initial time when operating power is turned on is held in the non-volatile memory.

50. A memory system according to Claim 42, wherein:

the non-volatile memory and the dynamic random access memory have the similar memory size; and

the static random access memory has memory size equal to/smaller than 1/1000 of that of the non-volatile memory.

51. A memory system according to Claim 44, wherein:

data transfer range data showing a range of a predetermined address region of the non-volatile memory is held in the non-volatile memory.

52. A memory system according to Claim 42, wherein:

the data-hold operation of the dynamic random access memory is executed inside the memory module.

53. A memory system according to Claim 51, wherein:

in case data-hold operation is applied to the dynamic random access memory from the device outside the memory module, the data-hold operation of the dynamic random access memory inside the memory module is stopped.

54. A memory system according to Claim 42, wherein:

access from the device outside the memory module is first preceded;

the data-hold operation of the dynamic random access memory inside the memory module is second preceded; and

data transfer between the non-volatile memory and the static random access memory or the dynamic random access memory is third preceded.

55. A memory system according to Claim 42, wherein:

the dynamic random access memory is synchronous DRAM; and

access to the non-volatile memory and the dynamic random access memory from the device outside the memory module is made via an interface of synchronous DRAM.

56. A memory system according to Claim 42, wherein:

the non-volatile memory is a NAND flash memory; and

the dynamic random access memory is synchronous DRAM.

57. A memory system according to Claim 42, wherein:

the non-volatile memory is an AND flash memory; and

the dynamic random access memory is synchronous DRAM.

58. A memory system according to Claim 42, wherein:

the non-volatile memory performs error detection, error correction and address replacement.

59. A memory system according to Claim 58, wherein:

a memory array of the non-volatile memory is configured

according to NAND configuration.

60. A memory system according to Claim 58, wherein:

a memory array of the non-volatile memory is configured according to AND configuration.

61. A memory system according to Claim 42, wherein:

the dynamic random access memory is equipped with plural interfaces.

62. A memory system according to Claim 61, wherein:

the plural interfaces with which the dynamic random access memory is equipped are interfaces for accessing at least two types of different memories.

63. A memory system according to Claim 61, wherein:

the interfaces with which the dynamic random access memory is equipped are the dynamic random access memory interface and the non-volatile memory interface.

64. A memory system according to Claim 42, wherein:

the dynamic random access memory is equipped with a control circuit for processing access from the device outside the memory module and a control circuit for independently accessing the non-volatile memory.

65. A memory system according to Claim 42, wherein:

the dynamic random access memory is equipped with a control circuit for independently accessing the non-volatile memory and a circuit for subordinately processing the access.

66. A memory system according to Claim 65, wherein:

the dynamic random access memory can select independent access to the non-volatile memory or subordinately processing the access.

67. A memory system according to Claim 42, wherein:

the non-volatile memory is equipped with the static random access memory, an error detecting and correcting circuit and an address replacement circuit.

68. A memory system, comprising:

a memory module including a non-volatile memory, a dynamic random access memory, a static random access memory and a control circuit that accesses the non-volatile memory, the dynamic random access memory or the static random access memory; and

an information processing device, wherein:

the information processing device performs data transfer to/from the static random access memory and the dynamic random access memory in the memory module via the dynamic memory interface.

69. A memory system according to Claim 68, wherein:

the information processing device reads a boot program from a boot program region of the static random access memory in the memory module via an SRAM interface in an initialization period immediately after power is turned on.

70. A memory system according to Claim 68, wherein:

in a normal period, the information processing device accesses the dynamic random access memory in the memory module

via the dynamic random access memory interface; and

in the normal period, the information processing device accesses a buffer region of the static random access memory in the memory module via a static random access memory interface.

71. A memory system according to Claim 68, wherein:

the information processing device instructs data transfer between the dynamic random access memory and the non-volatile memory in the memory module via the dynamic random access memory interface; and

the information processing device instructs data transfer between a buffer region of the static random access memory and the non-volatile memory in the memory module via a static random access memory interface.

72. A memory system according to Claim 68, wherein:

in a period when reading, writing, a refresh instruction and other instructions from the information processing device to the memory module are not executed in the memory module, data transfer between the dynamic random access memory and the non-volatile memory is performed; and

in the period, data transfer between the static random access memory and the non-volatile memory is performed.

73. A memory system according to Claim 42, wherein:

the non-volatile memory is formed in a first semiconductor chip;

the dynamic random access memory includes the control

circuit and the static random access memory and is formed in a second semiconductor chip; and

the first and second semiconductor chips are a multichip memory module mounted on a circuit board and packaged.

74. A memory system according to Claim 68, wherein:

the non-volatile memory is formed in a first semiconductor chip;

the dynamic random access memory includes the control circuit and the static random access memory and is formed in a second semiconductor chip;

the information processing device is formed in a third semiconductor chip; and

the first to third semiconductor chips are a multichip memory module mounted on a circuit board and packaged.

75. An information device configured by an information processing device, a memory device and an output device, wherein:

the memory device is the memory system according to Claim 1.

76. An information device configured by an information processing device, a memory device and an output device, wherein:

the information processing device and the memory device are the memory system according to Claim 31.

77. An information device configured by an information processing device, a memory device and an output device, wherein:

the memory device is the memory system according to Claim

42.

78. An information device configured by an information processing device, a memory device and an output device, wherein:

the information processing device and the memory device are the memory system according to Claim 68.